In the Claims:

This listing of claims replaces all previous listings and versions of claims in the application.

1. (Cancelled)

2. (Currently amended) A delay line comprising at least two four-transistor delay units connected in series, wherein a four-transistor delay unit ~~, comprising:~~ consists of

a first amplifier having a first and a second transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor is connected to a drain of the second transistor and a gate of the second transistor is connected to a drain of the first transistor; and

a second amplifier having a third and a fourth transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals, wherein a differential input voltage is connected to gates of the second amplifier transistors, a power supply voltage controlling the delay is connected to sources of the first amplifier and the delay unit uses substantially all available power supply voltage.

3. (Currently amended) A delay line comprising at least one delay unit, ~~comprising:~~ the delay unit consisting of

a first amplifier having a first and a second transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor is connected to a drain of the second transistor and a gate of the second transistor is connected to a drain of the first transistor;

a second amplifier having a third and a fourth transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals, wherein a differential input voltage is connected to gates of the second amplifier transistors, a power supply voltage controlling the delay is connected to sources of the first amplifier and the delay unit uses substantially all available power supply voltage; and

a fifth and a sixth transistor connected in parallel with the first and second transistor, the gates of the fifth and sixth transistor connected to their drains.

4. (Cancelled)

5. (Currently amended) A four-transistor differential controlled delay unit, ~~comprising:~~ consisting of

a first amplifier having a first and a second transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor is connected to a drain of the second transistor and a gate of the second transistor is connected to a drain of the first transistor, and the first amplifier transistors are NMOS transistors; and

a second amplifier having a third and a fourth transistor, wherein a drain of the third and fourth transistors is connected to a drain of the first and second transistors to form output terminals, wherein the second amplifier transistors are PMOS transistors, a differential input voltage is connected to gates of the third and fourth transistors, a supply voltage is connected to the sources of the second amplifier, and wherein a delay period is determined by the supply voltage and the delay unit uses substantially all available supply voltage, and wherein the NMOS transistors have a width-to-length ratio of greater than 30 and the PMOS transistors have a width-to-length ratio of greater than 40.

6. (Previously presented) A delay line comprising at least two of the four-transistor delay units according to Claim 5 connected in series.

7. (Currently amended) A voltage controlled oscillator, comprising:

a first delay unit and a second delay unit, each ~~further comprising~~ delay unit consisting of four transistors, said delay units each having a first amplifier having a first and a second transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor is connected to a drain of the second transistor and a gate of the

second transistor is connected to a drain of the first transistor, said delay units each having a second amplifier having a third and a fourth transistor,

wherein a drain of the third and fourth transistors is connected to a drain of the first and second transistors, said connections forming output terminals of the delay unit, and

wherein output terminals of the first delay unit are connected to gates of the second amplifier of the second delay unit, and output terminals of the second delay unit are connected to gates of the second amplifier of the first delay unit, and wherein a power supply voltage is connected to sources of the first amplifiers.

8. (Original) The voltage controlled oscillator of Claim 7, wherein the transistors for the first amplifiers are PMOS transistors and the transistors for the second amplifiers are NMOS transistors.

9. (Original) The voltage controlled oscillator of Claim 7, wherein a positive supply voltage is connected to the first amplifiers and a negative supply voltage or ground is connected to the second amplifiers.

10. (Previously presented) The voltage controlled oscillator of Claim 7, further comprising an additional delay unit.

11. (Previously presented) The voltage controlled oscillator of Claim 7, wherein the transistors for the first amplifiers are PMOS and the transistors for the second amplifiers are NMOS and a drain of the first and second transistors is connected to a drain of the third and fourth transistors to form outputs of the delay units.

12. (Previously presented) The voltage controlled oscillator of Claim 11, further comprising an additional delay unit.

13. (Previously presented) The voltage controlled oscillator of Claim 7, wherein in the first delay unit and the second delay unit, drains of the first amplifier are connected to drains of the second amplifier to form output terminals,

and wherein the output signals of the first delay unit are connected to gates of the second delay unit, and output signals of the second delay unit are connected to gates of the first delay unit, and wherein the power supply voltage is connected to sources of the first and second delay units.

14. (Previously presented) The voltage controlled oscillator of Claim 13, further comprising an additional delay unit, wherein output signals from the second delay unit are connected to gates of the additional delay unit, and output signals of the additional delay unit are connected to gates of the first delay unit.

15-16. (Cancelled)

17. (Previously presented) The voltage controlled oscillator of Claim13, wherein the transistors of the first amplifiers are PMOS and the transistors of the second amplifiers are NMOS.

18. (Original) The voltage controlled oscillator of Claim 7, further comprising a charge pump and a buffer, wherein a buffered output voltage of the charge pump is a supply voltage to the first amplifiers.

19. (Original) The voltage controlled oscillator of Claim 7, further comprising at least one additional delay unit, wherein output terminals of a delay unit are connected to gates of a next delay unit, and output terminals of a last delay unit are connected to the gates of the first delay unit.

20-23. (Cancelled)